Patterning of nanometer-scale cantilevers integrated in CMOS circuit by e-beam lithography

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Nano-electromechanical systems are based on the advantages of miniaturizing mechanical structures, such as cantilevers, for obtaining enhance functionality. NEMS represents an outcome of MEMS technology, scaled down to submicron dimensions. In this size regime, it is possible to attain extremely high fundamental frequencies while simultaneously preserving a very high mechanical response (small force constants). This powerful combination of attributes translates directly into high force sensitivity, operability at ultra-low power, and the ability to induce usable nonlinearity with quite modest control forces. Further development of NEMS requires surpassing several challenges which have to be addressed from a multidisciplinary framework that includes physicists, chemists, biochemists, and electrical and mechanical engineers. One of the aspects that offer more interest is the integration of NEMS with CMOS electronic circuits. Realization of nano/micro systems based on such combination offers an optimal path for interfacing the nanostructure to the external connections; it allows on-chip signal processing and permits the management of arrays of nanodevices.

In this work, we have evaluated the use of e-beam lithography (EBL) for the definition of silicon nanocantilevers in a pre-patterned CMOS substrate. The final objective is to develop a mass sensor with a sensitivity in the range10^{-17}-10^{-19} g [1, 2]. Deposition of mass onto the cantilever results in a decrease of its resonance frequency. The cantilever is driven at this resonance frequency by means of applying an oscillating voltage between the cantilever and an electrode located at a sub-micron separation. The detection of the oscillation of the cantilever is performed by amplifying the displacement current through the cantilever. As the equivalent capacitance of the cantilever/electrode system is extremely small (in the fF range), integration of the cantilever into a CMOS circuit reduces the contribution of the extra parasitic capacitance of pads and external wires that would hide the signal.

EBL allows higher resolution on the definition of the cantilever. When the dimensions of the cantilevers decrease, the mass sensitivity increases because the relative change of mass increases and the thermo-mechanical noise reduces [3]. The definition of the cantilever starts after completing the CMOS circuit fabrication. The cantilever is fabricated in a specific area (figure 1). The structural layer is the polysilicon bottom layer of the CMOS. Desirable characteristics of this layer are small surface roughness and a thickness of around 600 nm. For this, a protection layer (top polysilicon) is previously deposited for protection during the CMOS fabrication. Eventually, removal of the top polysilicon induces some damage that degrades surface roughness and thickness.

Other constraints that appear when EBL is performed on CMOS substrates are: i) It is necessary to use low energy electrons to reduce the damage on the circuit; ii) the alignment of the pattern in the pre-defined area has to be made without a previous SEM inspection; iii) The topography of the CMOS circuit presents steps of several microns which difficult the uniformity of the resist deposition, the focusing of the e-beam and the correct patterning near the edges of the steps. These constraints have been soften by defining pre-contacts by UV lithography as it is shown in figure 2. Preliminary examples of the cantilever definition are presented in figure 3.

Acknowledgments
This work has been partially funded by the project NANOSYS (MCYT-TIC2003-0723)

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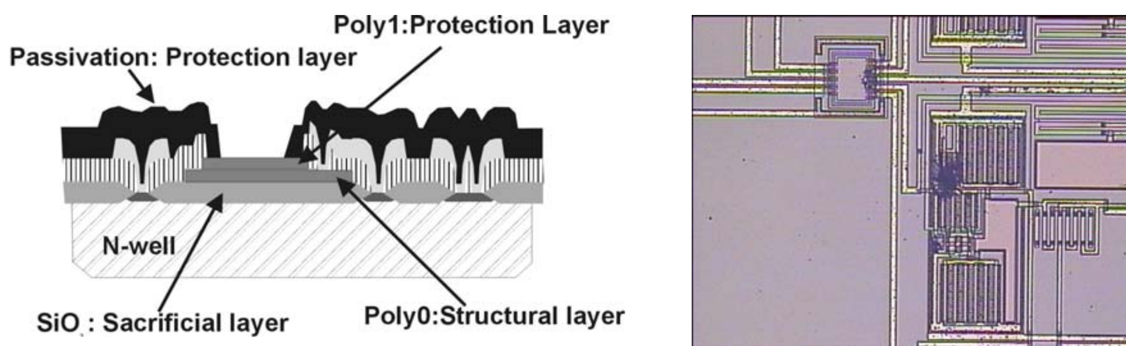

Figure 1. Left: Schematic cross section of the fabrication area after CMOS. The 2nd polysilicon layer (poly1) of the technology, is used during CMOS to protect the structural layer (poly0). It is removed by RIE, befor nanofabrication process. Right: Optical image fo one part of the chip showing the circuit and the area for fabrication

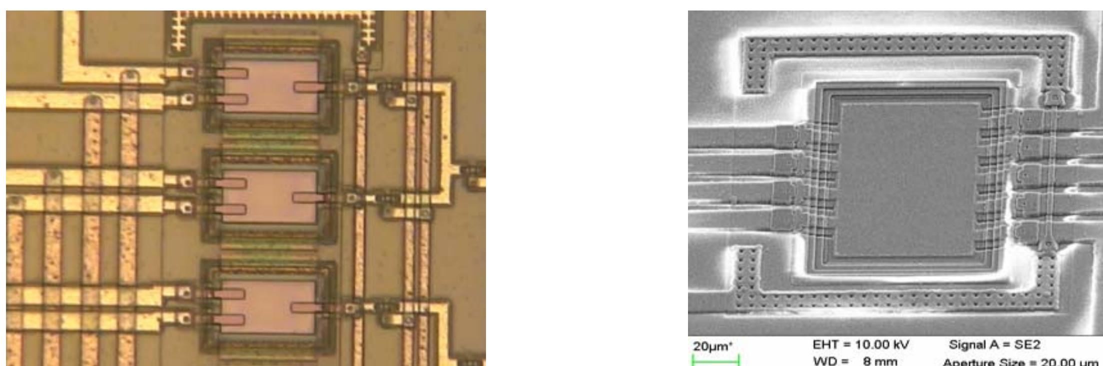

Figure 2. Left: optical image of a section of an array of areas in the CMOS circuit prepared for the fabrication of th enanocantilevers. Eelctrical contacts has been defined by UV lithography to make easy the alignemnt and the patterning of the edges. Right: SEM mage of another area prepared for fabricating a packed array of 4 cantilevers. It shows the topography of the area

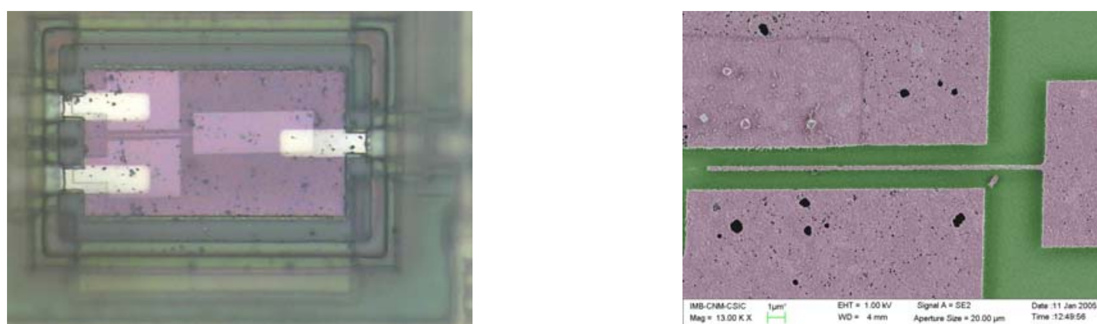

Figure 3. Left: Optical image after the e-beam exposure, development, deposition of 24 nm of aluminum and lift-off. Right: Colorful SEM image of a cantilever after the etching of silicon and under-etching of the silicon oxide to release the cantilever. The width of the cantilever is 200 nm.